REMARKS

Claims 4 and 5 were rejected under 35 U.S.C. 102(b) as being anticipated by Upp.

In claim 4, Applicants claim "reading, by the receiver block, of the data signal with a ***different sampling period than the transmission period*** of the transmitter block" (emphasis added). The Examiner asserts that this feature is taught by Upp due to the presence of "asynchronous devices." The Examiner points to Upp Figure 4 and col. 5, lines 5-11. Applicants respectfully traverse.

First, Upp concerns asynchronous data transfer, but it is clear from Figures 1 and 2 that the bus master and the various bus users all share a common system clock (SCLOCK), system clock frame (SCFRAME) and data clock (DCLOCK). In fact, the bus master supplies both the system clock (SCLOCK) and the system clock frame (SCFRAME) to all of the bus users. There is accordingly clock coordination and synchronous timed clock operation among all of the components of the Upp system. There Examiner's assertion of "asynchronous devices" being present is accordingly not understood, since there is a master clock and frame timing shared by the devices. In view of the foregoing, Applicants submit that the Examiner's technical analysis of the cited Upp reference is incorrect. The existence of a shared master clock and frame timing would more likely indicate a SAME transmit and receive sampling periods. This is contrary to the claimed invention.

Second, even with some asynchronous data transfer operations in Upp, this would not require that the transmit period be different from the receive sampling period, and Upp certainly does not explicitly recite that the transmit period and receive sampling period is different. In order to anticipate, the cited reference must explicitly or inherently teach all of the claim limitations. In this case, it is clear that there is no explicit teaching for the claimed different transmit and receive sampling periods. Applicants disagree that there is any inherent teaching for the claimed different periods due to the asynchronous operation. If the Examiner believes that such an operation is inherent in Upp, then Applicants traverse and request that the Examiner provide a reference proving that systems with shared master clock and frame timing as taught by Upp would have to operate with different transmit and receive sampling periods.

In view of the foregoing, Applicants request that the Section 102 rejection of claims 4 and 5 be withdrawn.

Claims 2, 3, 14, 16, 17, and 25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of Cagenius.

Turning first to claims 2, 14 and 25, Applicants claim that the synchro signal is delayed with respect to the data signal. The Examiner correctly concedes that this is not taught by Upp. The Examiner instead relies on Cagenius. Applicants respectfully disagree.

Cagenius is concerned with determining transmission delay. The Cagenius reference does not teach purposefully delaying the communication of the synchro signal with respect to the data signal. Rather, Cagenius is concerned with determining a signal transmission delay. These transmission delays can then be compensated for by advancing the time for initiating transmission of the data (see, for example, col. 3, lines 44-67). Thus, Cagenius fails to teach the claim limitation, as previously recited in claim 2 for example, "wherein said synchro signal is delayed for communication over the third line with respect to the data signal which is communicated over the first line."

In an effort to advance prosecution, and clarify what is meant by a delay, Applicants have amended claim 2 to recite that "generating said synchro signal for communication over the third line is delayed with respect to generating the data signal for communication over the first line." This amendment is made to clearly distinguish over the Cagenius delay determination, since the delay at issue in Cagenius is the delay for data receipt due to propagation delays encountered during signal transmission. Such propagation delays are clearly different from the claim 2 action to delay the generation of one signal for transmission with respect to the generation of another signal for transmission.

Claim 14 has been amended to recite "wherein transmitting from the transmitting entity comprises delaying sending the synchronization signal over the second communication line with respect to sending the data signal over the first communication line." The delayed sending of one signal with respect to the sending of another signal, as claimed, is quite different from Cagenius' operation to determine a signal propagation delay, and then account for that determined delay by advancing the sending of a signal with respect to other signals.

Claim 25 has been amended to recite that "the sending of the active synchronization signal transmission over the third communication line is delayed with respect to sending of the data signal transmission on the first communication line." Again, Cagenius does not teach or suggest that the sending of one signal be delayed with respect to another signal, as claimed.

In view of the foregoing, Applicants submit that claims 2, 14 and 25 are patentable over the cited prior art.

Claims 6, 9, 10, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of the admitted prior art.

Claim 6 includes limitations relating to repeater stages and elementary delays. The Examiner concedes that these features are not taught by Upp, but asserts that such are recognized as admitted prior art in the background of this application. Applicants do recognize the use of repeaters as being in the prior art, but Applicants do not admit that the elementary delay configuration in known from or is inherent in the admitted prior art. Applicants accordingly traverse the rejection and request that the Examiner prove, with respect to the admitted prior art, that the "stages have an elementary delay which must be shorter than half the transmission period." Applicants further assert that choosing such an elementary delay is not an obvious matter of design choice. Accordingly, Applicants request that the Examiner provide a reference teaching the selection of the claimed elementary delay.

Claims 9 and 19 also include limitations relating to repeater stages. However, Applicants specifically claim that the tristate condition of the data and syncho repeaters is controlled by the tristate output of the congestion repeater. The repeaters shown in admitted prior art Figure 1 do not teach using the specifically claimed configuration for controlling data/syncho repeaters with the congestion repeater. As such, the prima facie rejection has not been satisfied. Withdrawal of the rejection to claims 9 and 19 is requested.

In view of the foregoing, Applicants submit that claims 6, 9, 10, and 19 are patentable over the cited prior art.

Claims 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Upp in view of Hann.

Claim 22 emphasizes the use of transmit/receive control lines in addition to data, synchro and congestion lines. The transmit/receive control lines specify which communications blocks are to function as transmitters and which are to function as receivers. Upp uses a bus arbitration and assignment protocol to assign transmit/receive functions to users based on request. The Examiner points to Upp's clock and ack lines as being transmit and receive signal lines, respectively. While these may be signal lines used for transmitting and receiving, Applicants claim language is more precise.

Specifically, claim 22 previously recited that these signal lines carry "control signals" which "specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal." The clock line provided by Upp does not specify which blocks are to be the transmit and receive blocks with respect to a data signal. Likewise, the ack line provided by Upp does not specify which blocks are to be the transmit and receive blocks with respect to a data signal. The Examiner must consider all of the material claim limitations, and in this case the Examiner's technical analysis fails to prove the existence of signal lines in Upp which "specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal."

Notwithstanding the foregoing, in an effort to advance prosecution, and clarify what is meant by the control signals on the transmit and receive signal lines, Applicants have amended claim 22 to recite that "the first and second communications blocks ***set a logic state of the transmit signal line and receive signal line*** which specify, for the bi-directional first communication line, which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal." The clock and ack lines in Upp are not set by the blocks to specify which block is to use the data line for transmission and which block is to use the data line for reception. Assignment of transmit/receive functionality in Upp is made through the bus arbitration and assignment protocol and the transmission of assignment data during a given clock cycle for a next frame

(see, col. 4, lines 38-48). There is no signal line in Upp whose logic state is set to specify transmit/receive assignment.

In view of the foregoing, Applicants submit that claims 22 and 23 are patentable over the cited prior art.

Applicants respectfully submit that the application is now ready for allowance.

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Respectfully submitted,

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